Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10. (canceled)

11. (canceled)

12. (canceled)

13. (canceled)

14. (canceled)

15. (canceled)

16. (canceled)

17. (canceled)

18. (canceled)

19. (currently amended) A phase-locked loop comprising:

a voltage controlled oscillator (VCO); and

a frequency detector in signal communication with said VCO, said frequency detector including:

a counter configured to receive:

a VCO signal from said VCO; and

a preset value; and

a controller operable to control said counter;

wherein said counter generates frequency information related to said VCO signal in response to said controller, said VCO signal, and said preset value;

wherein:

said controller is additionally configured to generate a preset signal and an enable signal to control said counter;

said controller generates said enable signal for a known time period in response to a reference clock;

said preset signal sets said counter to said preset value; and

said frequency information is generated by said VCO signal changing said counter over said known time period in response to said enable signal.

20. (canceled)

21. (currently amended) The phase-locked loop ~~frequency detector~~ of claim 19 wherein said preset value is selected such that the counter is at one-half full-

scale at the end of said known time period when the VCO signal is oscillating at a target frequency.

22. (currently amended) The phase-locked loop ~~frequency detector~~ of claim 19 further comprising deadband logic in signal communication with said counter, said deadband logic configured to determine whether the frequency of said VCO signal is controlled in response to a signal from said frequency detector or a signal from a phase detector.

23. (currently amended) The phase-locked loop ~~frequency detector~~ of claim 22 wherein said deadband logic is configured to use dual deadband values to determine whether the frequency of said VCO signal is controlled in response to said signal from said frequency detector or said signal from said phase detector.

24. (currently amended) The phase-locked loop ~~frequency detector~~ of claim 19 further including logic connected to ~~in signal communication with~~ said counter for providing different charging currents to said loop filter dependent on said frequency information from said counter.

25. (new) A phase-locked loop comprising:

a voltage controlled oscillator (VCO); and

a frequency detector in signal communication with said VCO, said frequency detector including:

a counter configured to receive:

a VCO signal from said VCO; and

a preset value; and

a controller operable to control said counter;

wherein said counter generates frequency information related to said VCO signal in response to said controller, said VCO signal, and said preset value;

wherein said preset value is selected such that the counter is at one-half full-scale at the end of said known time period when the VCO signal is oscillating at a target frequency.

26. (new) The phase-locked loop of claim 25 wherein:

said controller is additionally configured to generate a preset signal and an enable signal to control said counter;

said controller generates said enable signal for a known time period in response to a reference clock;

said preset signal sets said counter to said preset value; and

said frequency information is generated by said VCO signal changing said counter over said known time period in response to said enable signal.

27. (new) The phase-locked loop of claim 25 further comprising deadband logic in signal communication with said counter, said deadband logic configured to determine whether the frequency of said VCO signal is controlled in response to a signal from said frequency detector or a signal from a phase detector.

28. (new) The phase-locked loop of claim 27 wherein said deadband logic is configured to use dual deadband values to determine whether the frequency of said VCO signal is controlled in response to said signal from said frequency detector or said signal from said phase detector.

29. (new) The phase-locked loop of claim 25 further including logic connected to said counter for providing different charging currents to said loop filter dependent on said frequency information from said counter.

30. (new) A phase-locked loop comprising:

a voltage controlled oscillator (VCO); and

a frequency detector in signal communication with said VCO, said frequency detector including:

a counter configured to receive:

a VCO signal from said VCO; and

a preset value; and

a controller operable to control said counter;

wherein said counter generates frequency information related to said VCO signal in response to said controller, said VCO signal, and said preset value;

deadband logic in signal communication with said counter, said deadband logic configured to determine whether the frequency of said VCO signal is controlled in response to a signal from said frequency detector or a signal from a phase detector.

31. (new) The phase-locked loop of claim 30 wherein:

said controller is additionally configured to generate a preset signal and an enable signal to control said counter;

said controller generates said enable signal for a known time period in response to a reference clock;

said preset signal sets said counter to said preset value; and

said frequency information is generated by said VCO signal changing said counter over said known time period in response to said enable signal.

32. (new) The phase-locked loop of claim 30 wherein said preset value is selected such that the counter is at one-half full-scale at the end of said known time period when the VCO signal is oscillating at a target frequency.

33. (new) The phase-locked loop of claim 30 wherein said deadband logic is configured to use dual deadband values to determine whether the frequency of said VCO signal is controlled in response to said signal from said frequency detector or said signal from said phase detector.

34. (new) The phase-locked loop of claim 30 further including logic connected to said counter for providing different charging currents to said loop filter dependent on said frequency information from said counter.